Homework

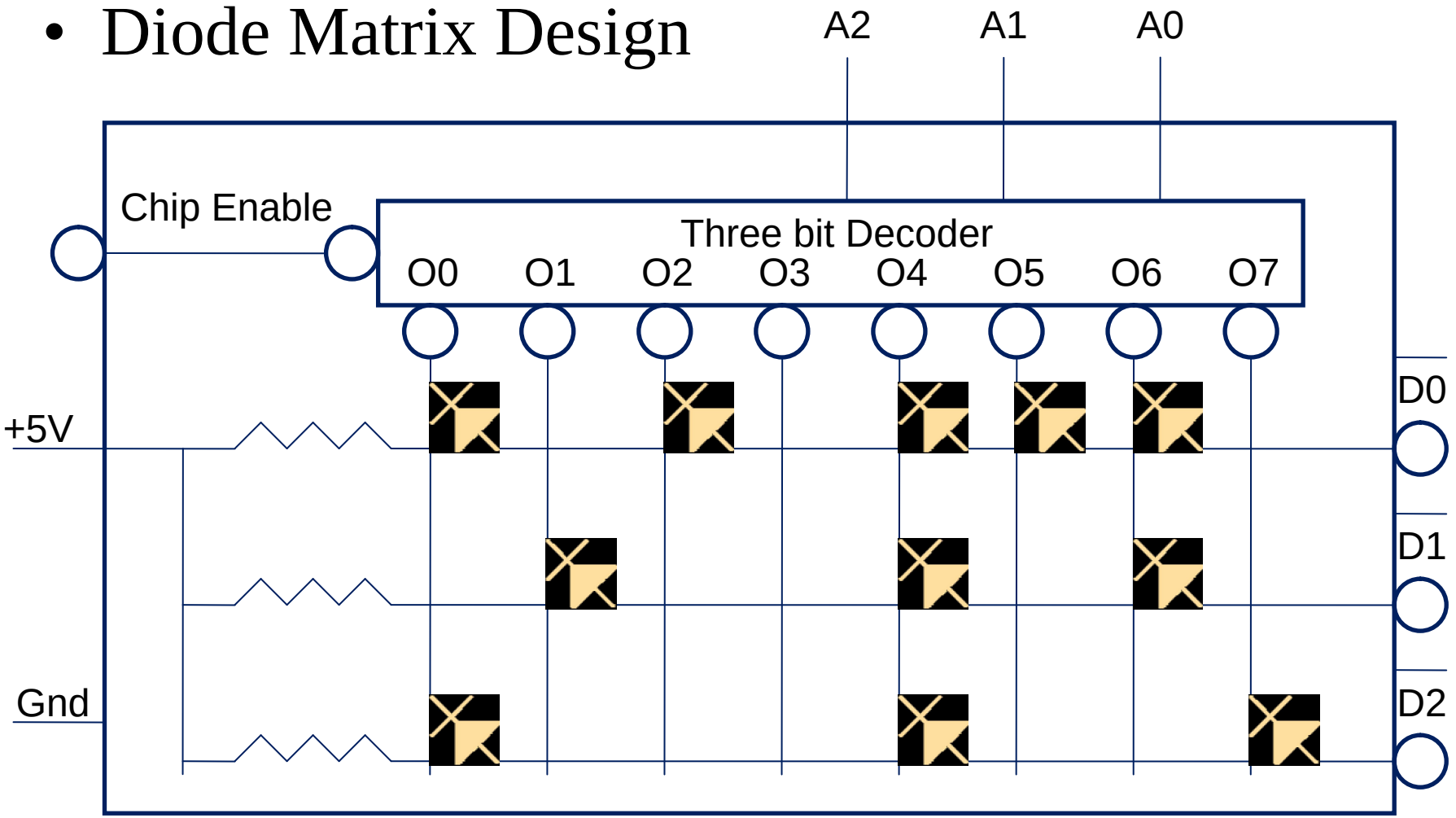
- Reading
  - Tokheim, Chapter 12-1 through 12-4
- Machine Projects
  - MP4 due at start of next class
- Labs
  - Continue with your assigned section

Read Only Memory (ROM)

- PC uses it to hold BIOS for system and I/O drivers
- Slow (100-200 nanoseconds)
- Various forms:
  - Read Only Memory (ROM)
  - Programmable Read Only Memory (PROM)
  - Erasable Programmable Read Only Memory (EPROM)
  - Electrically Erasable Programmable ROM (EEPROM)
  - Flash memory

Read Only Memory (ROM)

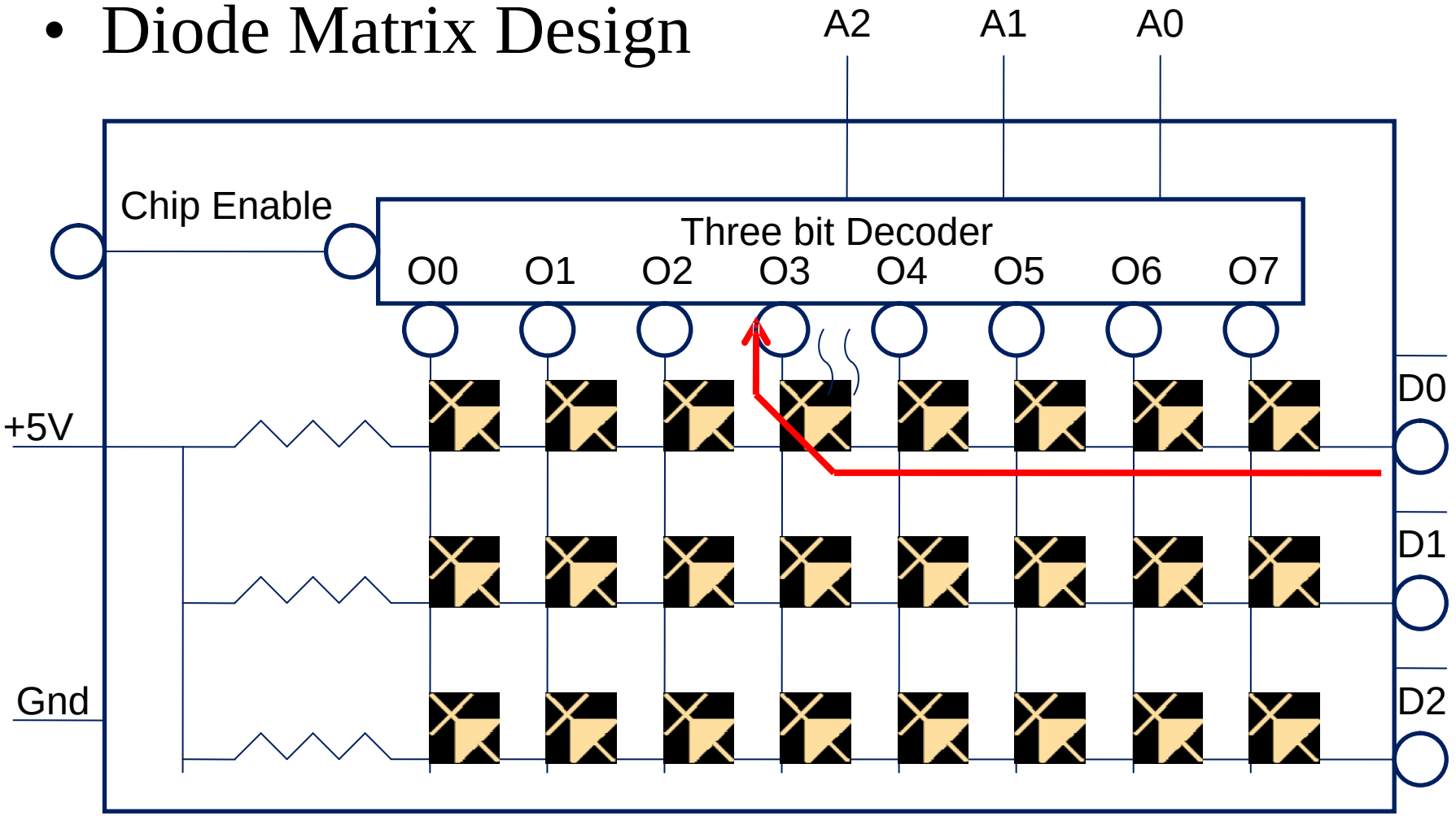
- Diode Matrix Design



Presence of a diode means a 1, absence of a diode = 0

Programmable ROM

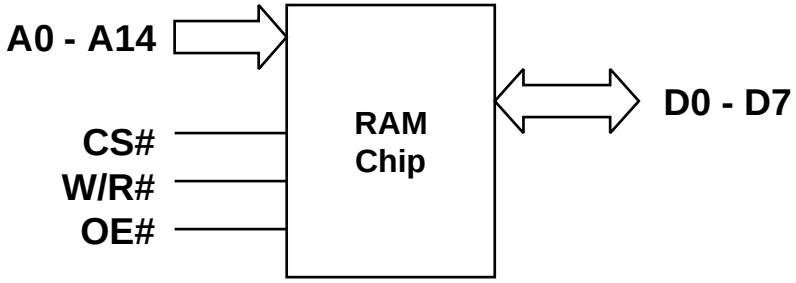
- Diode Matrix Design



Starts with all diodes/all ones. Burn out diodes where value needs to be zero.

Random Access Memory (RAM)

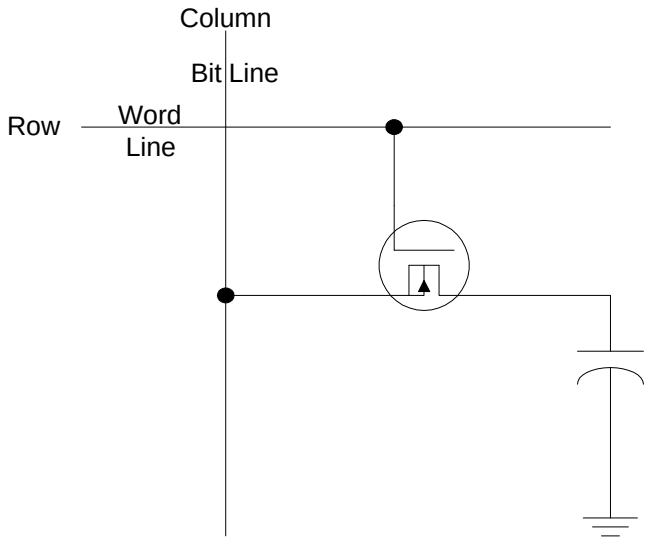
- Static RAM = an array of full flip-flops
- Simple interface and fast (10-20 nsec) but more costly (2 - 4X) than ROM



- Small capacity compared to Dynamic RAMs

Dynamic RAM (DRAM)

- Square array of simple one transistor memory cells
- Capacitance at input to transistor remembers a 0 or 1



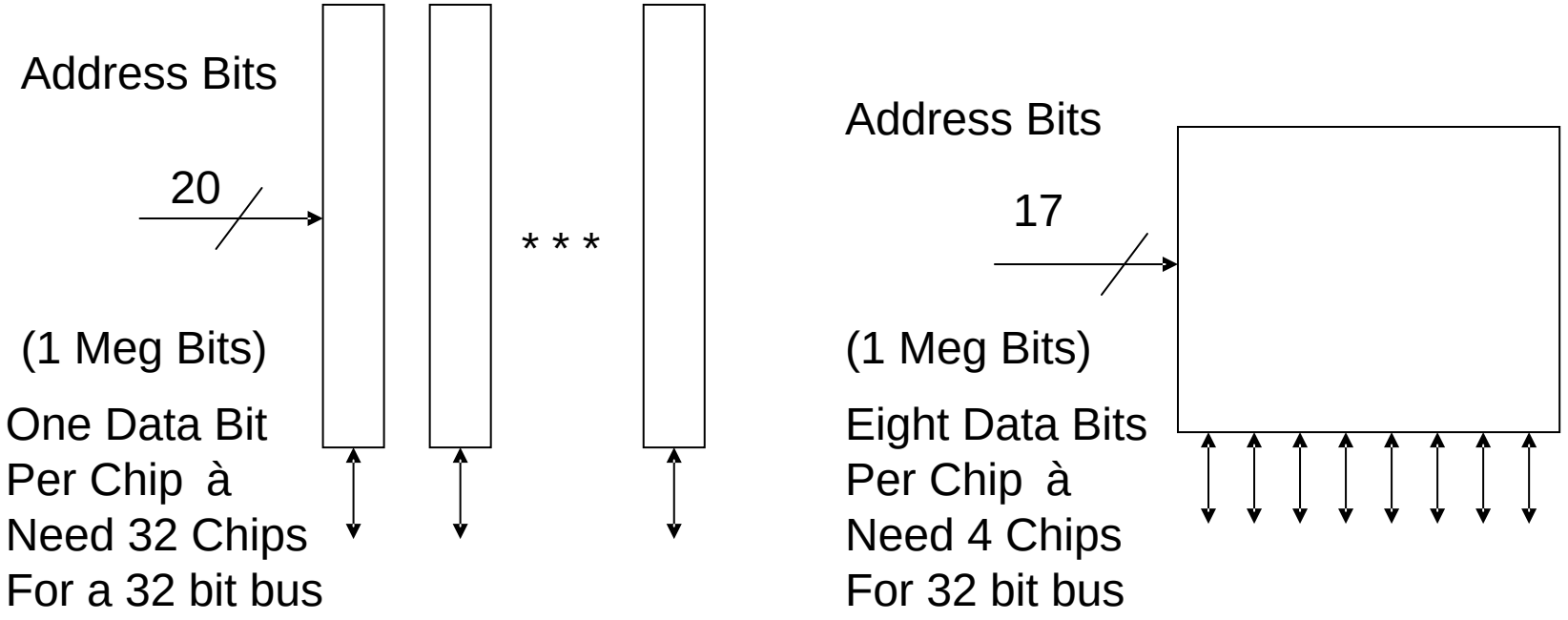
- Reading contents of the cell is destructive
- Over time, the charge leaks away (in milliseconds)

Dynamic RAM (DRAM)

- For both reasons, HW must perform a *memory refresh*
- Regularly reading/writing on a row and column basis
- Advantages are:
  - Cells are simple
  - Uses less power
- Disadvantage:
  - Slower (20 - 30 nsec access time)
  - Total cycle time is 2X due to refresh after read
- Bottom line
  - 2-4X less chip area and 2-4X less power
  - Interleaving and access in column or page mode

Example Layouts of Memory Parts

- Organized 1 Meg x 1 or Organized 128K x 8

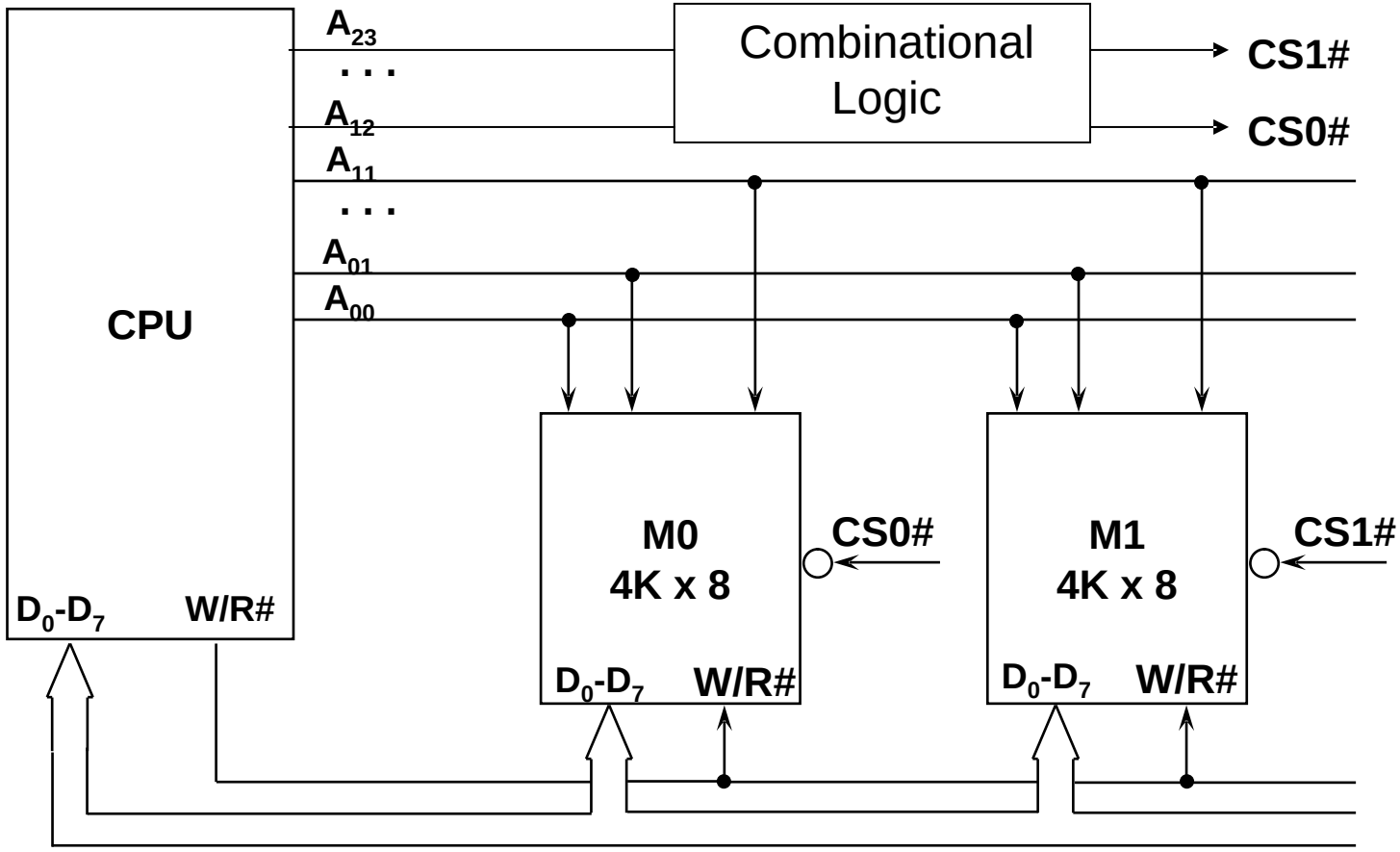


Number of Data Bit Pins Attached to Data Bus

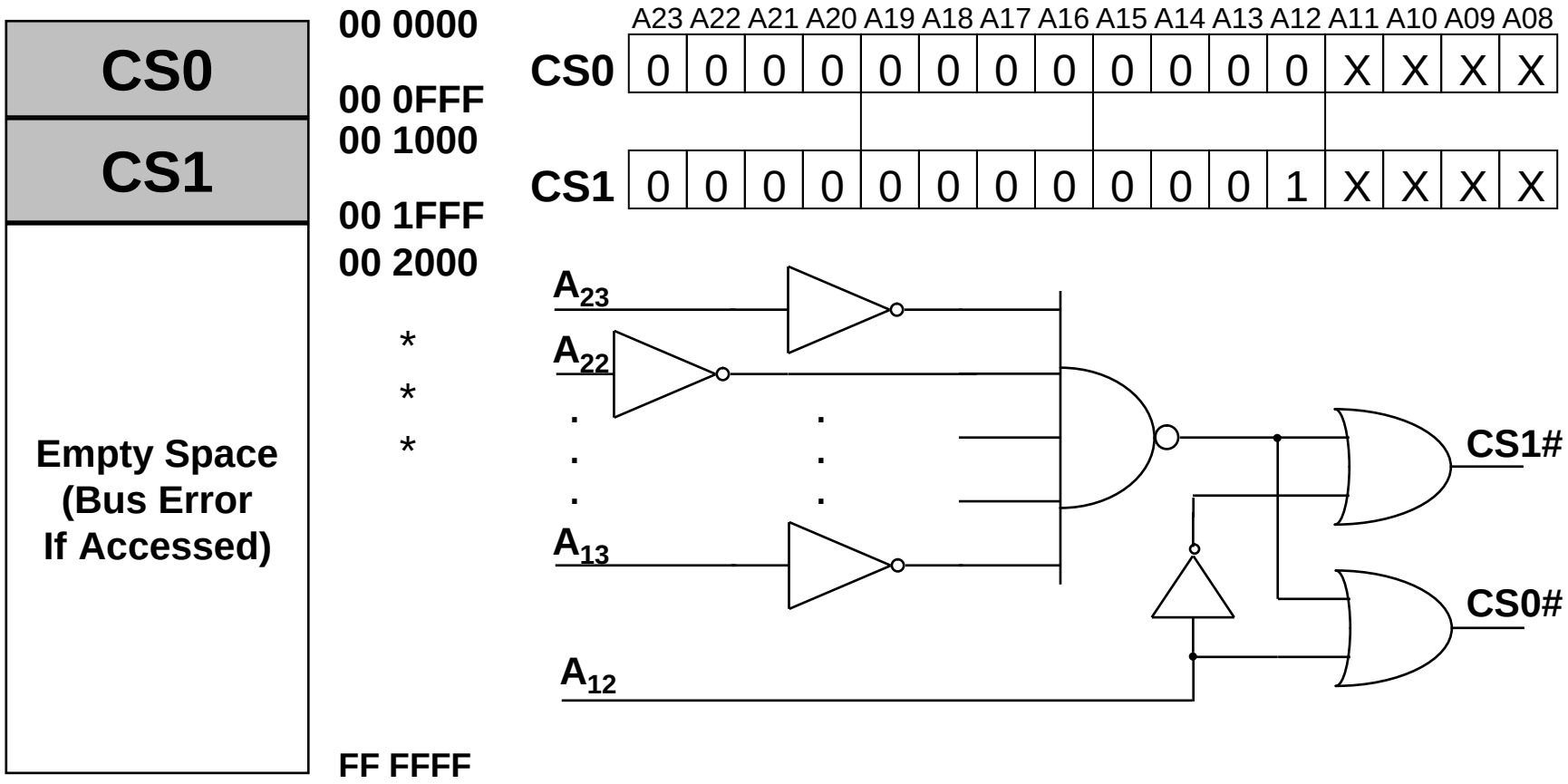
Full Address Decoding

- Each location within a memory component responds to only one unique address
- Need to use all the address lines in decoding
- May choose not to fill-in some portions of the address space with real memory (empty spots)

Addressing Memory Components



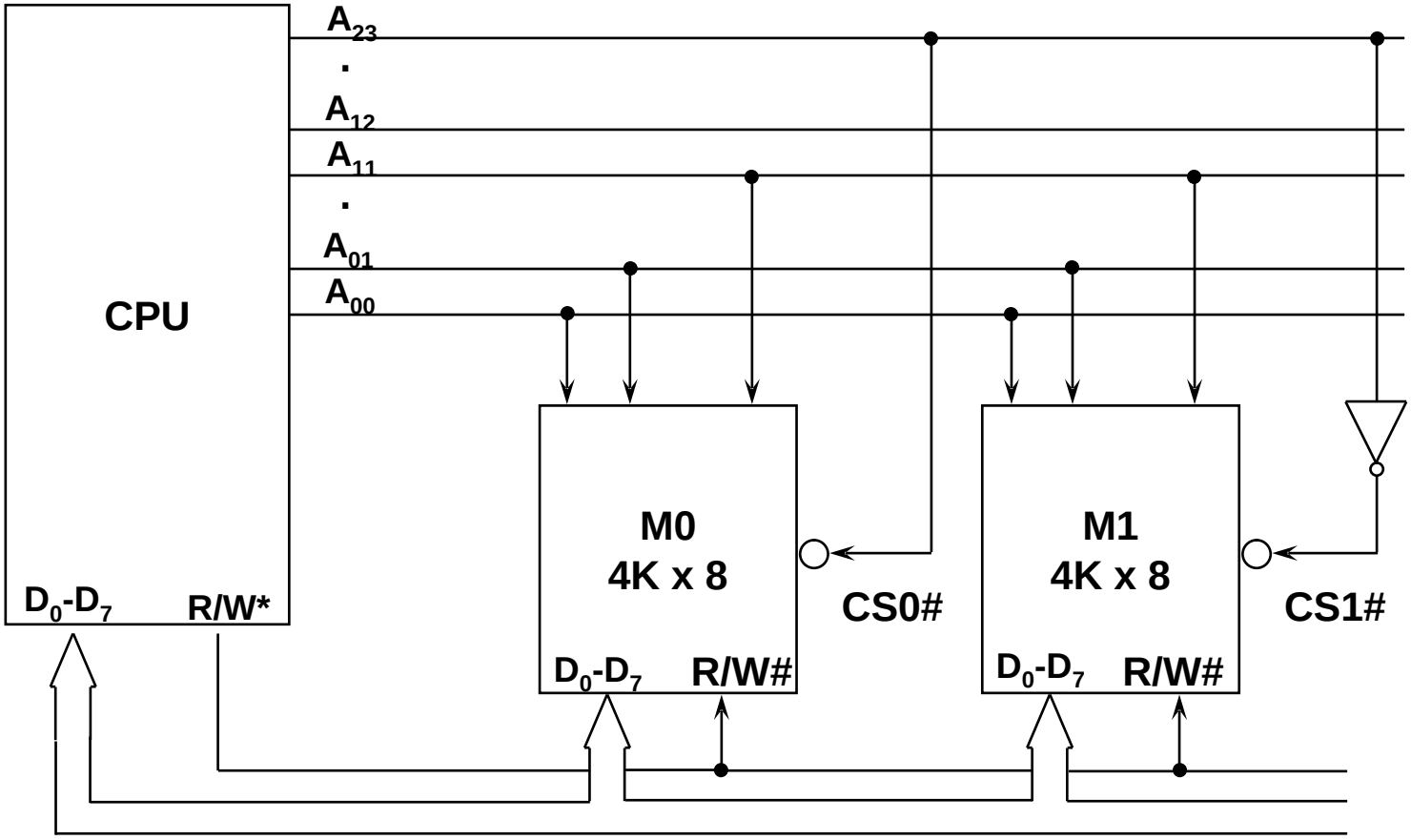
Memory Map and Comb. Logic



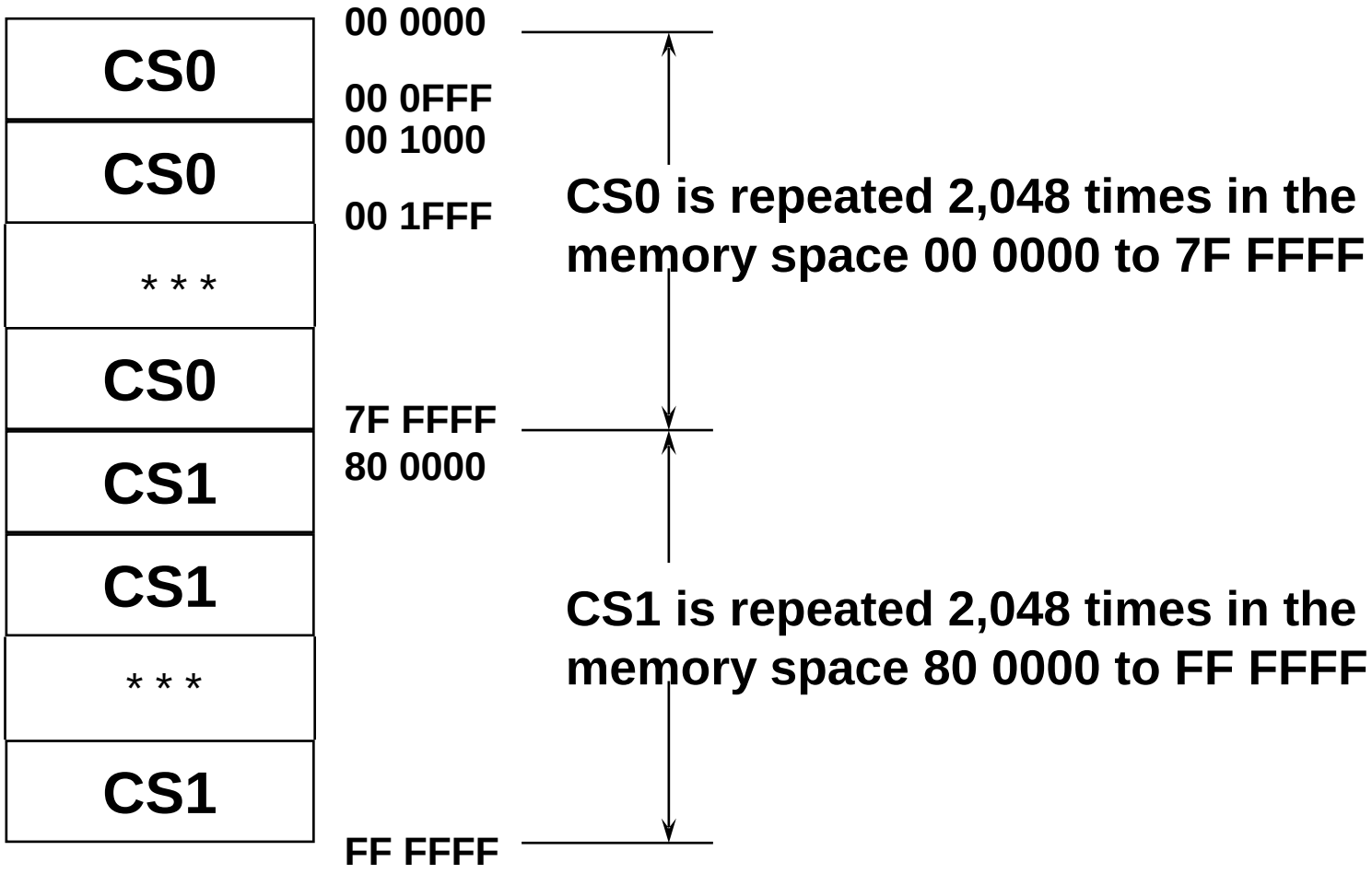
Partial Address Decoding

- Simpler and less expensive
- Some address lines are NOT used in the address decoding process to generate chip enable signals
- Many groups of addresses can map to the same physical memory chip

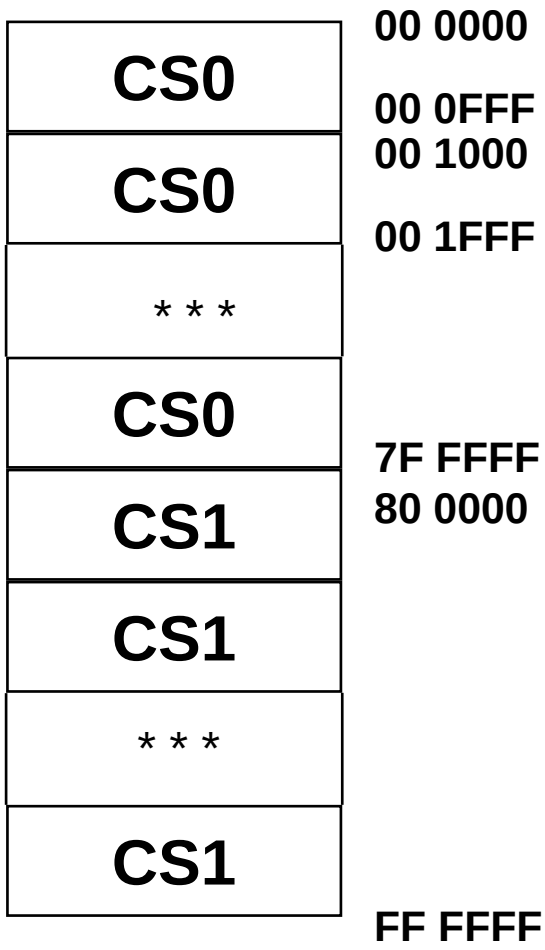
Partial Address Decoding

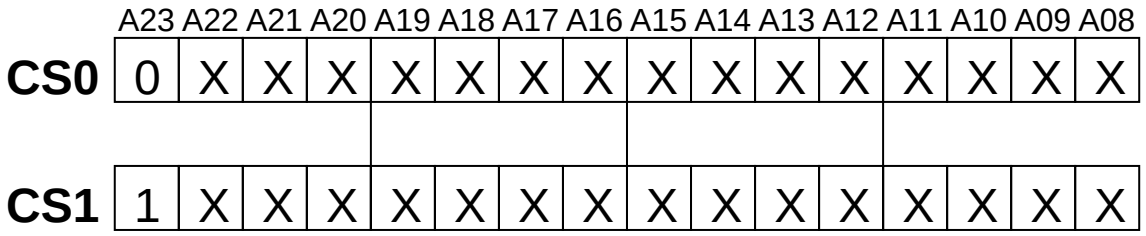


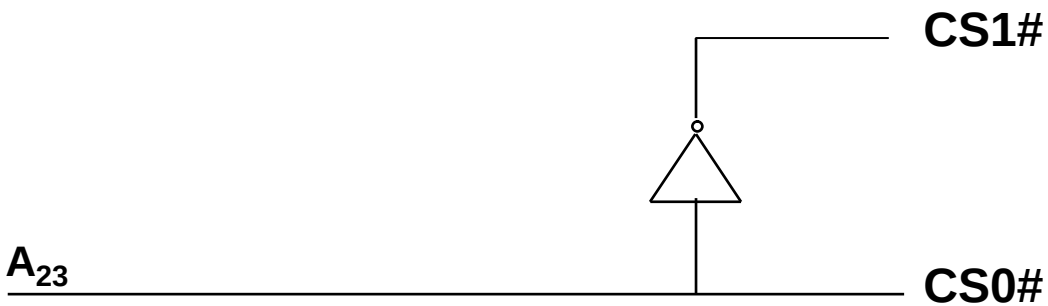
Memory Map for Partial Decoding



Comb. Logic for CS0 and CS1







Mixed Address Decoding

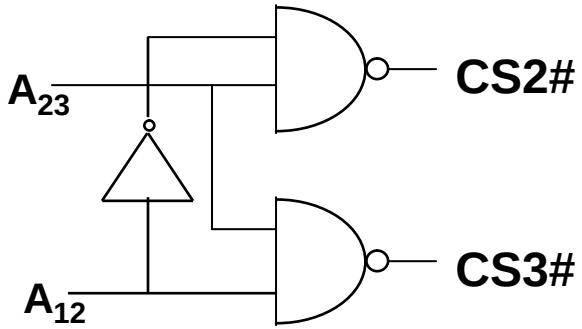
- A mixture or a compromise between partial and full address decoding
- Divide the memory space into a number of fully decoded blocks, generally of equal size
- Use high-order address bits to select the block and low-order address bits to select a sub-block

Comb. Logic for CS0, CS1, CS2, & CS3

	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08
CS0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
CS1	0	1	0	0	0	0	0	0	0	0	0	0	X	X	X	X

	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08
CS2	1	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X
CS3	1	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X

Logic Diagram for CS0# and CS1#
Similar to Diagram on Slide 11
Except A_{22} and A_{12} are swapped



Memory Map for Mixed Decoding