Homework

• Reading
  – None (Finish all previous reading assignments)

• Machine Projects
  – Continue with MP5

• Labs
  – Finish lab reports by deadline posted in lab
Hierarchy for 80286 Memory and I/O

- IBM PC-AT ("Advanced Technology" in 1984)
- DOS 3.0 Operating System
- PC-AT bus evolved into Industry Standard Bus
- Many manufacturers built ISA-based PCs/cards
- ISA Bus
  - Slow 6 MHz evolved to 8 MHz or 125 nsecs/cycle
  - Address Bus 20 bits
  - Data Bus 16 bits
IBM PC-AT

Big Picture (80286)

ISA Bus: 20/16 bits, 8 MHz (125 nsecs/cycle)
Hierarchy for 80486 Memory and I/O

• CPU Clock: 66 MHz
• Local Bus or CPU Bus
  – “Fast” 33MHz / 32 bits wide
• Expansion Bus Controller (CPU-ISA Bridge)
• ISA Bus (Legacy)
  – “Slow” 8 MHz or 125 nsecs/cycle
  – Address Bus 20 bits
  – Data Bus 16 bits
Big Picture (80486)

- **CPU**
  - Local bus or CPU bus: fast (33 MHz, 32 bits) [30 nsec./cycle]
  - Memory
  - Cache
  - Video Adapter
  - Disk
  - Expansion Bus Controller

- **System ROM**
  - ISA bus: slow (8 MHz, 8/16 bits) [125 nsec./cycle]
  - RTC
  - Keyboard
  - Serial Port
  - Parallel Port
  - Floppy Disk
Competition for ISA replacement

- Many vendors proposed busses to replace ISA as the technology improved
  - IBM: Micro Channel Architecture (MCA)
  - Extended Industry Standard Architecture (EISA)
  - VESA Local Bus
  - Intel: Peripheral Component Interconnect (PCI)
- PCI had won commercial battle by mid-90’s
- For a while PCs had a mix of ISA and PCI slots
Hierarchy for Pentium 4 Memory and I/O

- **CPU Clock Speed**
  - “Fast” 2 – 2.5 GHz

- **CPU “Front End” Bus Speed**
  - “Fast” 533 MHz / 64 bits wide evolved to 800 MHz

- **CPU-PCI Bridge (“North Bridge”)**

- **PCI Bus (Most prevalent peripheral bus after ISA)**
  - “Medium Speed”: 33 or 66 MHz / 32 or 64 bits wide

- **PCI-ISA Bridge (“South Bridge”)**

- **ISA Bus (Most prevalent “Legacy” peripheral bus)**
  - “Slow Speed”: 8 Mhz / 20 and 16 Bits
The Big Picture (Pentium)

Pentium CPU

CPU bus: fast (100 MHz, 64 bits) [10 nsec./cycle]

Cache

PCI Controller

Memory

PCI bus: fast (33 MHz, 32/64 bits) [30 nsec./cycle]

Video Adapter

Disk

System ROM

Expansion Bus Controller

ISA bus: slow (8 MHz, 8/16 bits) [125 nsec./cycle]

RTC

Keyboard

Serial Port

Parallel Port

Floppy Disk

“North Bridge”

“South Bridge”
Motherboard Chipsets

- The motherboard chip set provides the core logic and manages the motherboard's functions.
- Several companies (including ATI, Intel, and nVidia) make motherboard chip sets, most of which offer the same basic features.
- The variants of nVidia's nForce4 chip set were the most widely used on the boards though Intel's 975X Express has become increasingly popular for Intel-based motherboards.
North Bridge

Expansion Bus Controller (CPU-PCI)
South Bridge

Expansion Bus Controller (PCI-ISA)

PCI Bus

- FRAME#
- TRDY#
- IRDY#
- STOP#
- REQ#
- GNT#
- AD[31:0]
- C/BE#[3:0]

ISA Bus

- MEMR#
- MEMW#
- IOR#
- IOW#
- INTA#
- A23-A0
- D23-D0

CLK
Pentium 4 CPU Specifications

• The Pentium 4 Processor
  – Introduced: May 6, 2002
  – 512KB level-two cache
  – Operating at 533 MHz “front side bus” speed
  – Available now at 2.53 GHz, 2.4 GHz and 2.26 GHz and is priced at $637, $562 and $423, respectively, in 1,000-unit quantities.
  – Benchmarks: SPECint*_base2000 score of 882
    SPECfp*_base2000 score of 860
  – "Springdale" will have a FSB speed of 800 MHz
Pentium CPU Block Diagram
Enhancing Performance

• “Pipelining is an implementation technique in which multiple instructions are overlapped in execution”, (Patterson and Hennessey, “Computer Organization and Design”, p. 436)

Sequential Execution:

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Pipeline Example (Cont’d)

• Pipelining improves the overall performance by *increasing instruction throughput per unit time* *not decreasing execution time of an individual instruction*

• Ideal speedup is number of stages in the pipeline

• Do we achieve this? Sometimes / Not always
  - Notice the idle time in the pipe at certain times
  - Flushing pipeline during conditional jumps
  - Data being calculated by previous instruction may be needed too early in the next instruction
Superscalar Processors

• More than one execution pipeline executing in parallel

• Note: Possible coordination problems must be resolved
Evolution of Computer Power

- Electronic Numerical Integrator and Computer (ENIAC) in 1946-47
  - 17,500 Vacuum Tubes
  - 7200 Crystal Diodes
  - 1500 Relays
  - 70,000 Resistors
  - 10,000 Capacitors
  - Five million hand soldered joints
  - Weighed 30 tons, took 1800 ft², 150 KWatts of power

- In 1995, 7.44mm x 5.29 mm, 20MHz chip
Moore’s Law

• Gordon Moore made a famous observation in 1965, just four years after the first planar integrated circuit was discovered
• Moore observed an exponential growth in the number of transistors per chip and predicted that this trend would continue
• Moore's Law, the doubling of transistors every couple of years, has been maintained, and still holds true today
Moore’s Law
Moore’s Law

1961 – 1st commercial chip. 4 transistors (Apollo spacecraft)

1974 – Intel 8080 5000 transistors (Altair PC)

2009 Intel Core i7 4 cores - 731 million transistors