

Homework

- Reading
 - None (Finish all previous reading assignments)
- Machine Projects
 - Continue with MP5
- Labs
 - Finish lab reports by deadline posted in lab
- Exam Next Class
 - Open book / open notes

Hierarchy for 80286 Memory and I/O

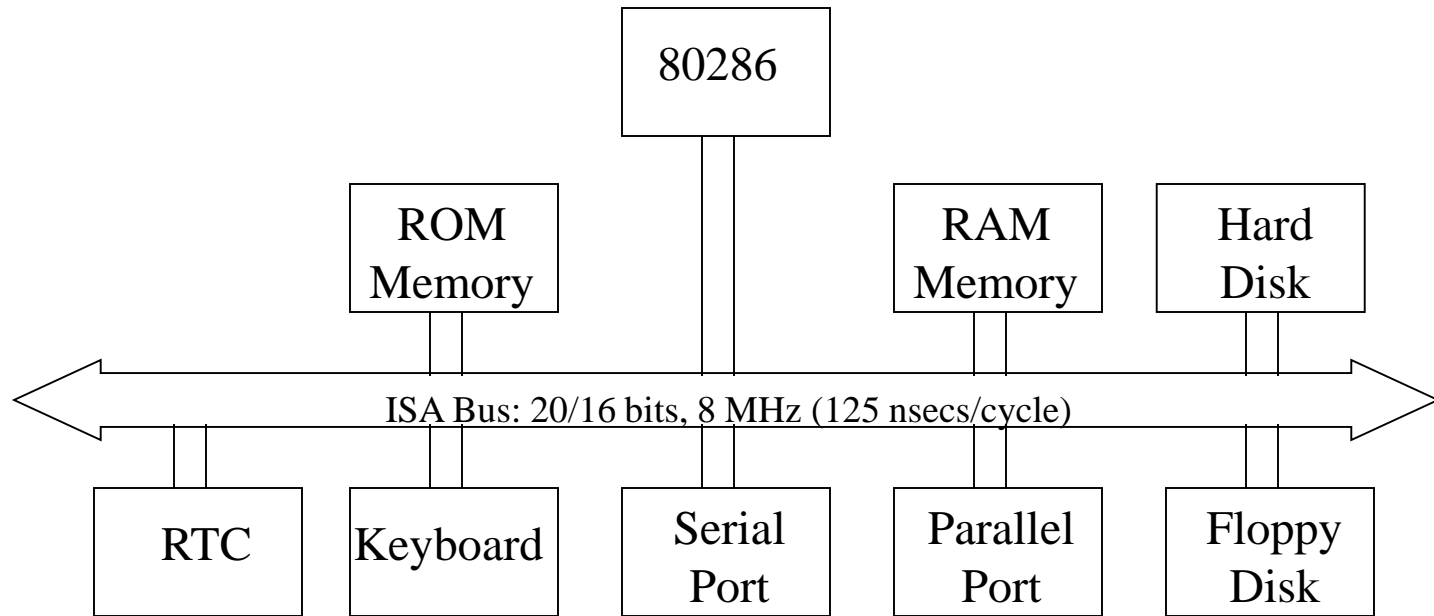
- IBM PC-AT (“Advanced Technology” in 1984)
- DOS 3.0 Operating System
- PC-AT bus evolved into Industry Standard Bus
- Many manufacturers built ISA-based PCs/cards
- ISA Bus
 - Slow 6 MHz evolved to 8 MHz or 125 nsecs/cycle
 - Address Bus 20 bits
 - Data Bus 16 bits

IBM PC-AT



Reference: <http://www.vintage-computer.com/ibmpcat.shtml>

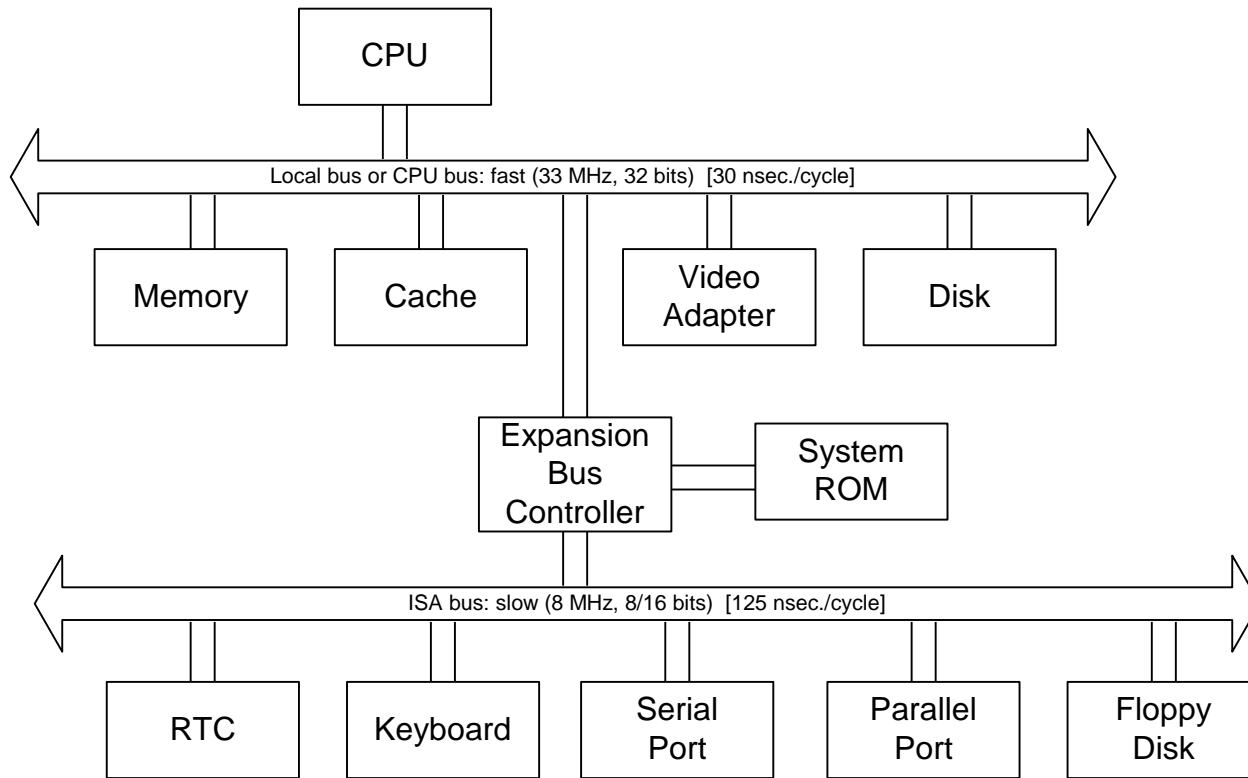
Big Picture (80286)



Hierarchy for 80486 Memory and I/O

- CPU Clock: 66 MHz
- Local Bus or CPU Bus
 - “Fast” 33MHz / 32 bits wide
- Expansion Bus Controller (CPU-ISA Bridge)
- ISA Bus (Legacy)
 - “Slow” 8 MHz or 125 nsecs/cycle
 - Address Bus 20 bits
 - Data Bus 16 bits

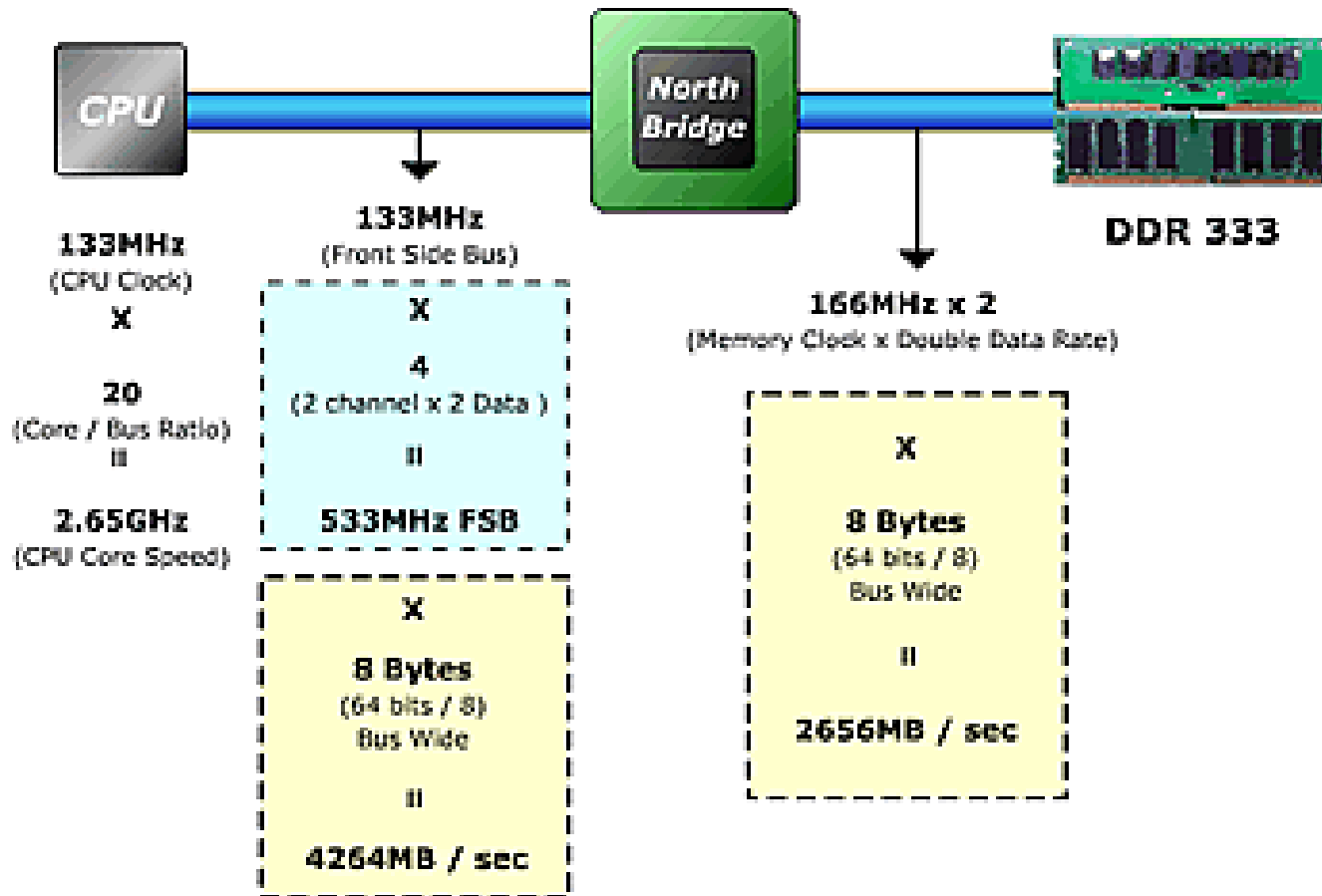
Big Picture (80486)



Competition for ISA replacement

- Many vendors proposed busses to replace ISA as the technology improved
 - IBM: Micro Channel Architecture (MCA)
 - Extended Industry Standard Architecture (EISA)
 - VESA Local Bus
 - Intel: Peripheral Component Interconnect (PCI)
- PCI had won commercial battle by mid-90's
 - “Medium Speed”: 33 or 66 MHz / 32 or 64 bits wide
- For a while PCs had a mix of ISA and PCI slots

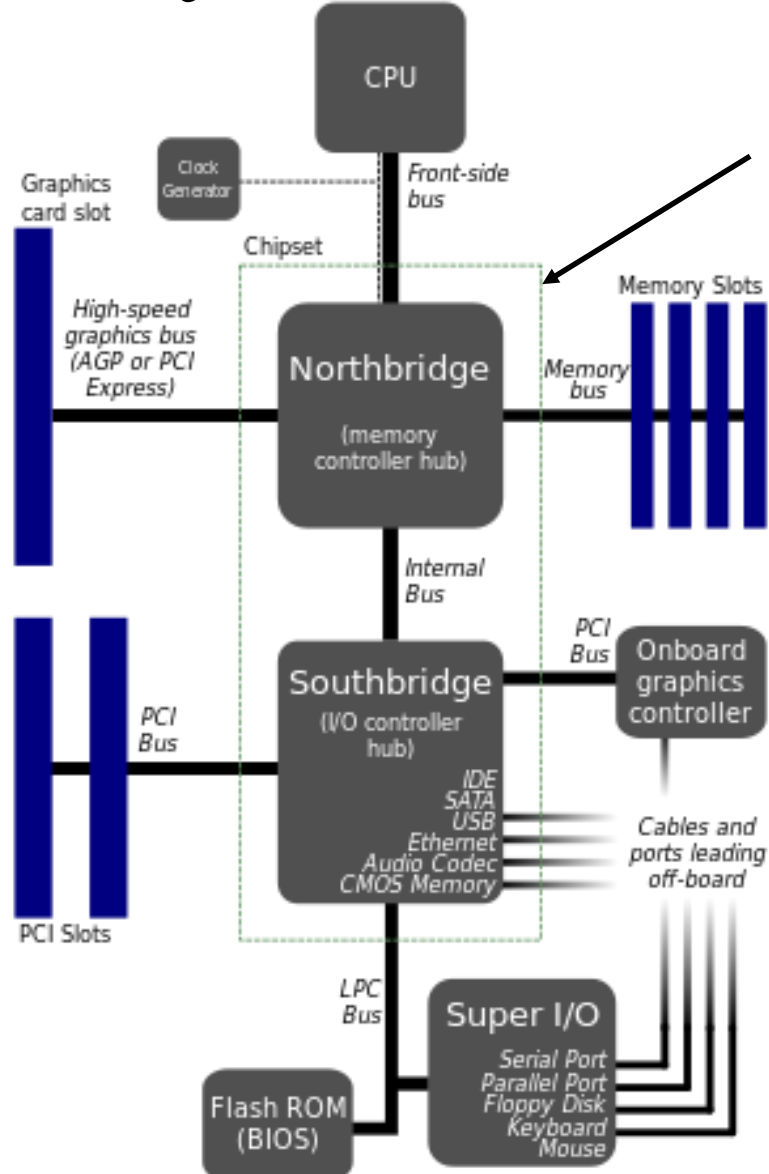
Hierarchy for Pentium Memory



Subsequent Evolution

- More and more of the “random logic” and VLSI chips surrounding the processor were included in Ultra-VLSI chips (“Motherboard chips”)
- The “North Bridge” allows highest speed access to program/data memory and high speed graphics processors (faster access than the PCI bus!)
- The “South Bridge” interfaces to PCI bus and incorporates devices for Ethernet, USB, etc.
- The Super I/O chip incorporates legacy interfaces
 - Floppy Disk, Keyboard, Parallel Port, Serial Ports, etc.

Hierarchy for Pentium Memory and I/O



Mother Board chip or chip set

Motherboard Chipsets

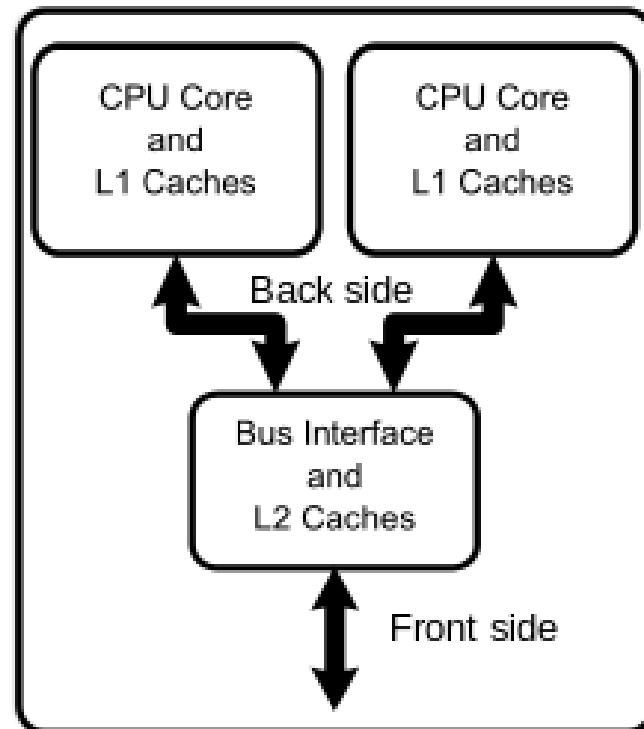
- The motherboard chip set provides the core logic and manages the motherboard's functions
 - CPU: CPU
 - NB: Northbridge
 - GPU: Graphics
 - SB: Southbridge



Source: Wikipedia

Multi-core CPU Chips

- To increase processing power, multiple CPU's are included in high performance CPU chips
- Example Dual core:



X86-64 Architecture

- **The x86-64** architecture is a 64-bit superset of the 32-bit x86 instruction set architecture
- x86-64 was designed by AMD who named it **AMD64**
- It has been cloned by Intel under the name **Intel 64**
- This leads to the vendor-neutral names *x86-64* or **x64**
- **Backward Compatible!** All instructions in the x86 instruction set can be executed by x86-64 CPUs
- x86-64 should not be confused with the Intel Itanium architecture known as *IA-64* which is not compatible at native instruction set level with x86 or x86-64

X86-64 Architecture

- Features
 - The number of named registers is increased from 8 (i.e. eax, ebx, ecx, edx, ebp, esp, esi, edi) to 16
 - All registers are expanded from 32 bits to 64 bits
 - All ALU, memory-to-register, and register-to-memory operations are now 64-bits wide
 - Pushes and pops on the stack are always in eight-byte strides, and pointers are eight bytes wide
 - Virtual memory address space up to 256 terabytes
 - Physical address space up to 1 terabyte

Intel/HP Itanium Processor

- **Intel Itanium architecture** (formerly called **IA-64**) originated at Hewlett-Packard and was later jointly developed with Intel
- This VLIW processor family has had limited success in servers and high performance computing systems
- Intel hoped it would also find broader acceptance as a replacement for the original x86 architecture
- That hasn't happened due to the success of x86-64 which has better backward compatibility with earlier x86 hardware and software
- Some people have critiqued Itanium as a failure

Moore's Law

- Gordon Moore made a famous observation in 1965, just four years after the first planar integrated circuit was discovered
- Moore observed an exponential growth in the number of transistors per chip and predicted that this trend would continue
- Later dubbed as “Moore's Law”, the doubling of transistors every couple of years, has been maintained, and still holds true today

Moore's Law - Originally

Gordon Moore's original graph, showing projected transistor counts, long before the term "Moore's law" was coined (Peter Bright, Feb 10, 2016)

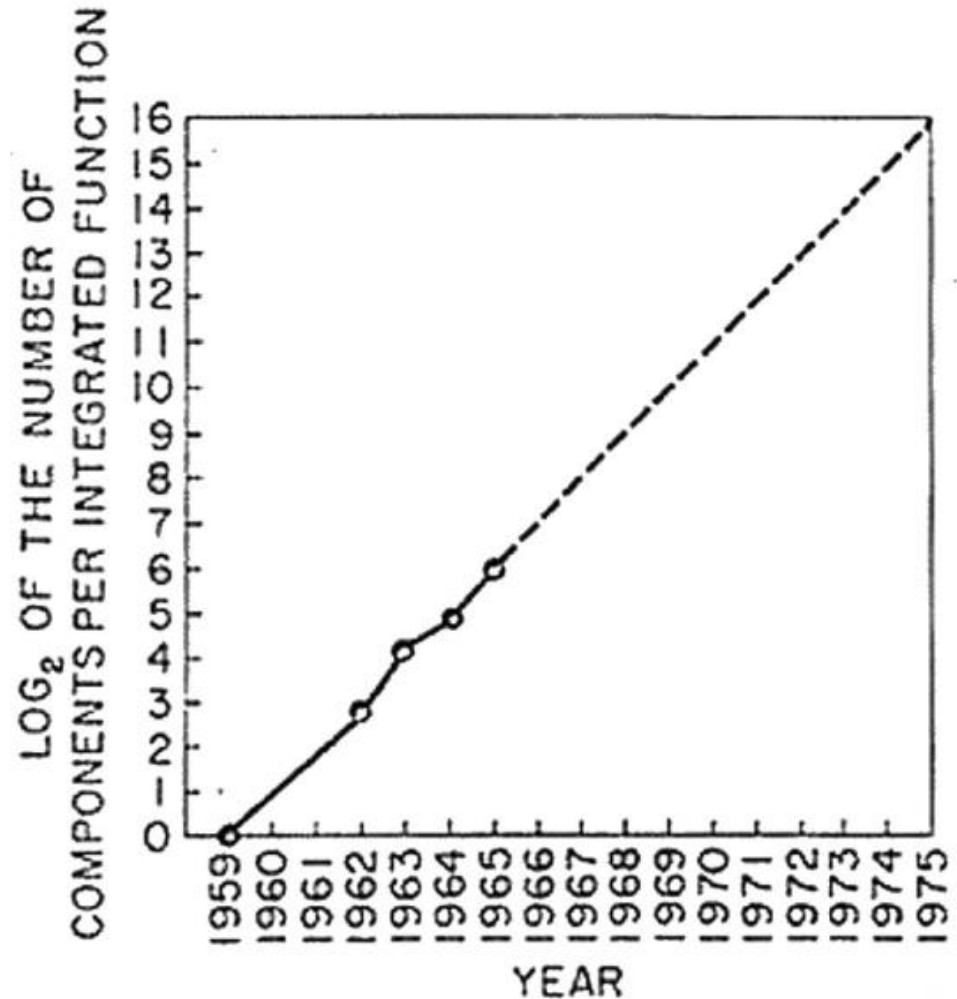
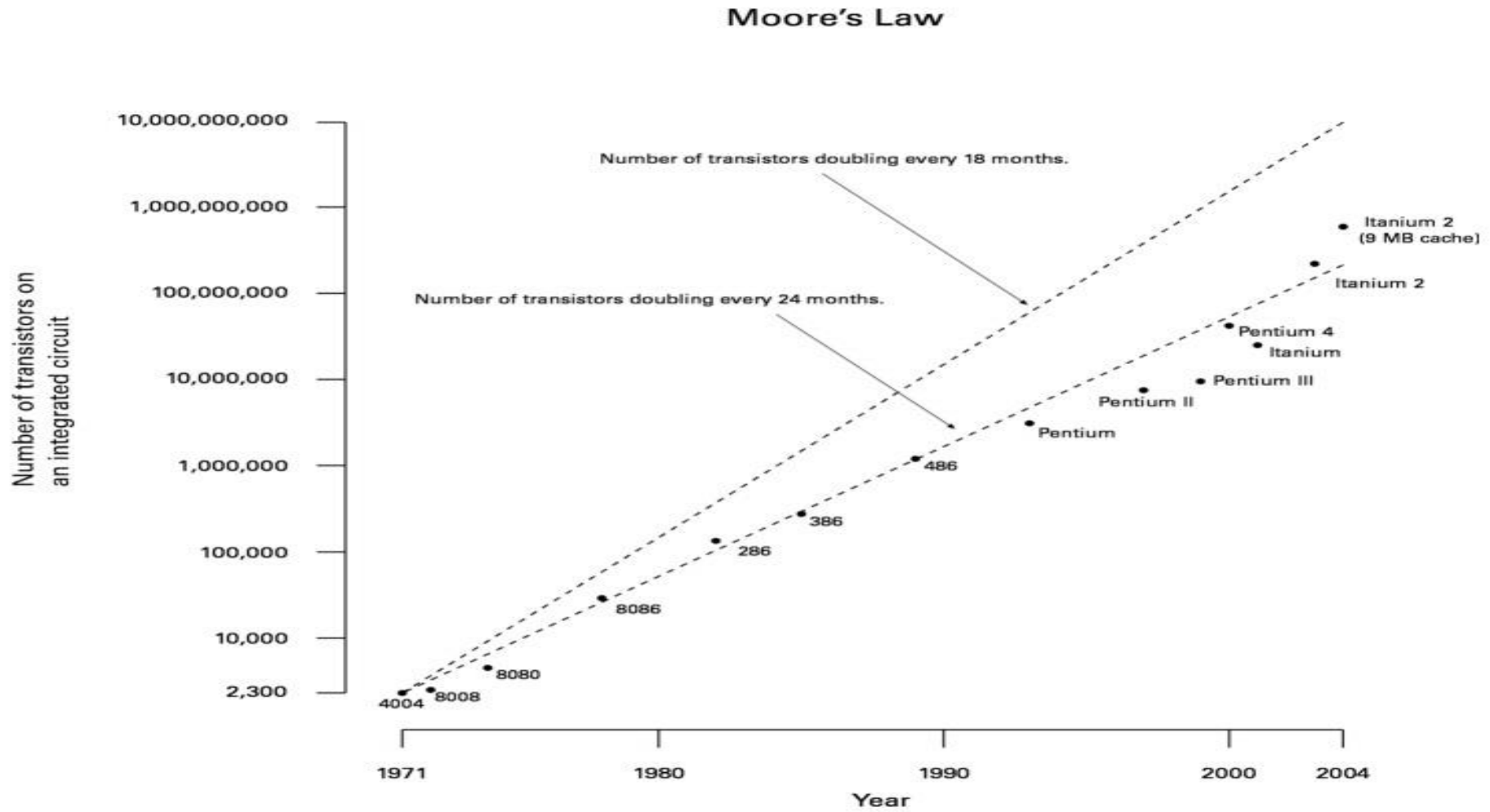
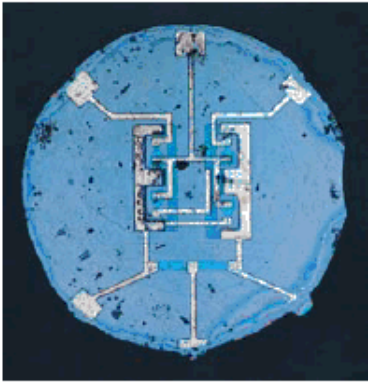


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

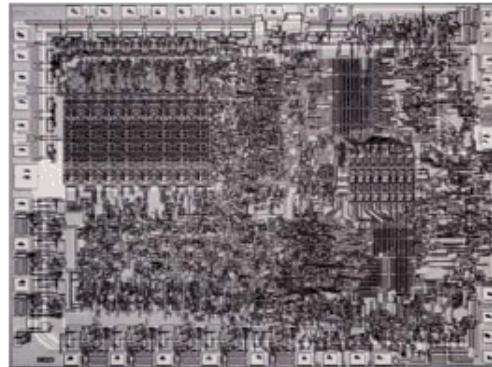
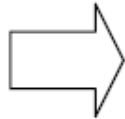
Moore's Law - More Recently



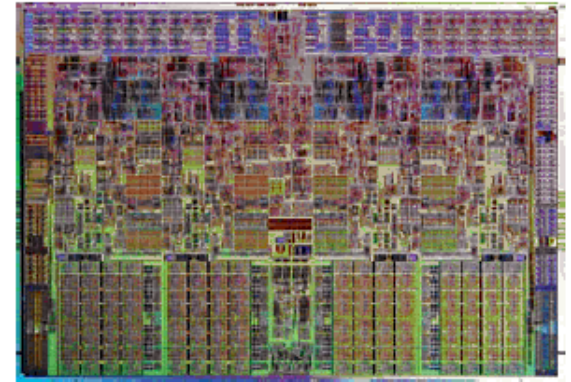
Moore's Law



**1961 – 1st
commercial chip.
4 transistors
(Apollo spacecraft)**



**1974 – Intel 8080
5000 transistors
(Altair PC)**



**2009 Intel Core i7
4 cores - 731 million
transistors**

Moore's Law Ending?

- There is some concern today that we are nearing the end of Moore's Law
- “Chip scientists are nearly at the point where they are manipulating material as small as atoms. When they hit that mark within the next five years or so, they may bump into the boundaries of how tiny semiconductors can become.”*

*Boston Globe, May 5, 2016