Software and Hardware

Outline

1. Representing Information
2. Boolean Functions
3. Logic Circuits
4. Von Neumann Architecture

Representing Information

Decimal (base 10) system

$$135 = \quad \cdot 10^2 + \quad \cdot 10^1 + \quad \cdot 10^0$$

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$$135 = 1 \cdot 10^2 + 3 \cdot 10^1 + 5 \cdot 10^0$$

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Binary (base 2) system

Decimal (base 10) system

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Binary (base 2) system

$$135 = \quad \cdot 2^7 + \quad \cdot 2^6 + \quad \cdot 2^5 + \quad \cdot 2^4 + \quad \cdot 2^3 + \quad \cdot 2^2 + \quad \cdot 2^1 + \quad \cdot 2^0$$

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Decimal (base 10) system

$$135 = 1 \cdot 10^2 + 3 \cdot 10^1 + 5 \cdot 10^0$$

Binary (base 2) system

$$135 = 1 \cdot 2^7 + 0 \cdot 2^6 + 0 \cdot 2^5 + 0 \cdot 2^4 + 0 \cdot 2^3 + 1 \cdot 2^2 + 1 \cdot 2^1 + 1 \cdot 2^0$$

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Octal (base 8) system

Decimal (base 10) system

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Octal (base 8) system

$$135 = 2 \cdot 8^2 + 0 \cdot 8^1 + 7 \cdot 8^0$$

Decimal (base 10) system

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Binary (base 2) system

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Hexadecimal (base 16) system

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$$135 = 8 \cdot 16^1 + 7 \cdot 16^0$$

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Dec	Bin	Oct	Hex
0	00000	00	00
1	00001	01	01
2	00010	02	02
3	00011	03	03
4	00100	04	04
5	00101	05	05
6	00110	06	06
7	00111	07	07
8	01000	10	08
9	01001	11	09
10	01010	12	0A
11	01011	13	0B
12	01100	14	0C
13	01101	15	0D
14	01110	16	0E
15	01111	17	0F

Dec	Bin	Oct	Hex
16	10000	20	10
17	10001	21	11
18	10010	22	12
19	10011	23	13
20	10100	24	14
21	10101	25	15
22	10110	26	16
23	10111	27	17
24	11000	30	18
25	11001	31	19
26	11010	32	1A
27	11011	33	1B
28	11100	34	1C
29	11101	35	1D
30	11110	36	1E
31	11111	37	1F

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Example (addition in binary)

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+ & 1 & 1 & 0 \\
\hline
\end{array}
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- Add 1 to the result to obtain 11111101

  Note: just like how $3 + (-3) = 0$, we have $00000011 + 11111101 = 100000000$

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- The last two digits for the exponent

Example: the 10-digit number 0314159001 represents $0.314159 \times 10^1 = 3.14159$

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The 16-bit Unicode system can represent every character in every known language, with room for more

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Example: the string “Python” is represented in decimal as the sequence

006 080 121 116 104 111 110

or in binary as the sequence

00000110 01010000 01111001 01110100 01101000 01101111 01101110

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- A picture as a sequence of triples, each containing the amount of red, green, and blue at a pixel
- A sound as a temporal sequence of “sound pressure levels”
- A movie as a temporal sequence of pictures (usually 30 per second), along with a matching sound sequence

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Truth tables for $\texttt{not}$, $\texttt{or}$, and $\texttt{and}$ functions

x	$\bar{x}$
0	1
1	0

x	y	$x + y$
0	0	0
0	1	1
1	0	1
1	1	1

x	y	$x \cdot y$
0	0	0
0	1	0
1	0	0
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0	1	1	
1	0	0	
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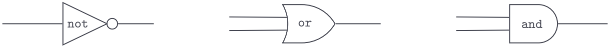
Ergo, $\texttt{implication}(x, y) = \bar{x} \cdot \bar{y} + \bar{x} \cdot y + x \cdot y$

Logic Circuits

Logic Circuits

The logic gates that implement the `not`, `or`, and `and` functions



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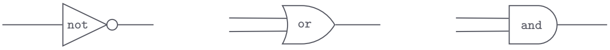
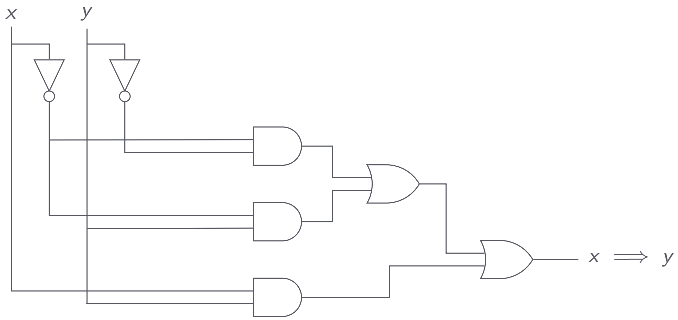
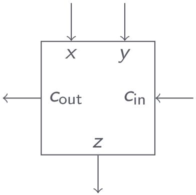


Logic circuit for the `implication` function $\bar{x} \cdot \bar{y} + \bar{x} \cdot y + x \cdot y$



Logic Circuits

A full adder (FA) circuit can add two 1-bit numbers (with carry) to produce a 2-bit result



x	y	c_{in}	z	c_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
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An n-bit ripple-carry adder is n FA circuits chained together to add two n-bit numbers

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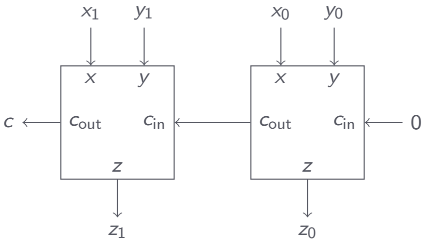
A 2-bit ripple-carry adder



Logic Circuits

Truth table for a nor gate (or followed by not)

x	y	$\overline{x+y}$
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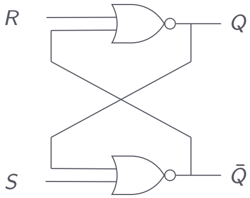

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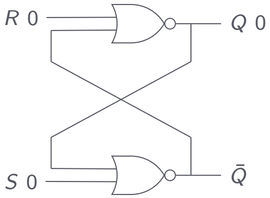

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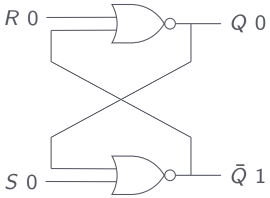

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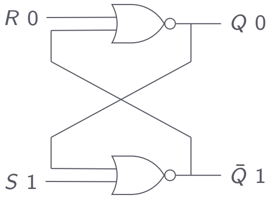

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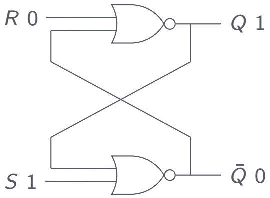

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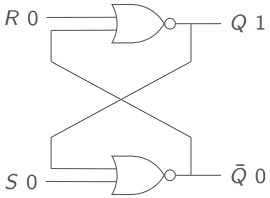

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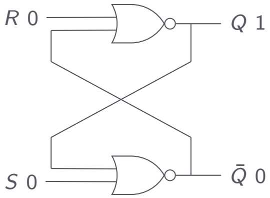

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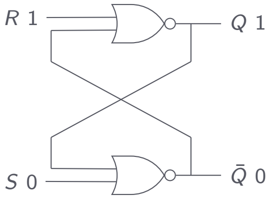

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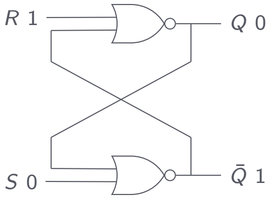

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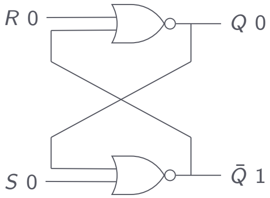

Logic Circuits

Truth table for a `nor` gate (`or` followed by `not`)

x	y	$\overline{x+y}$
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0	1	0
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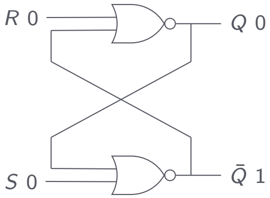

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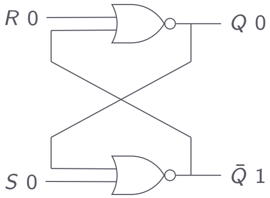

A billion latches can be combined together to produce a 1GB Random Access Memory (RAM) module

Von Neumann Architecture

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In a modern computer, the Central Processing Unit (CPU) is where all computation takes place

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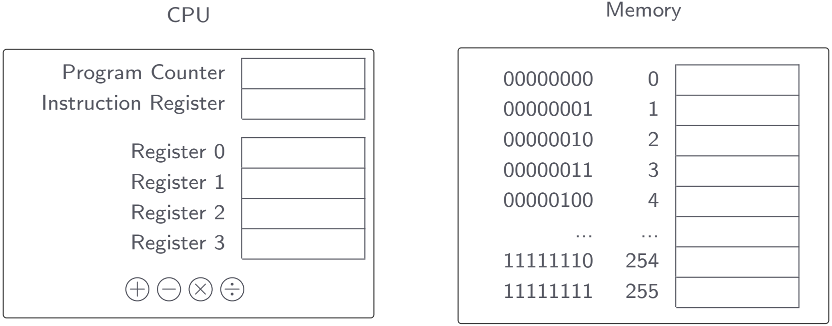
1. A program counter to track the next instruction to execute
2. An instruction register to store the next instruction for execution

Von Neumann Architecture

Example: an 8-bit computer with four operations (add, subtract, multiply, and divide), four registers (0 through 3), and 256 8-bit memory cells



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Instructions, like data, can be encoded as numbers

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add 2 0 1
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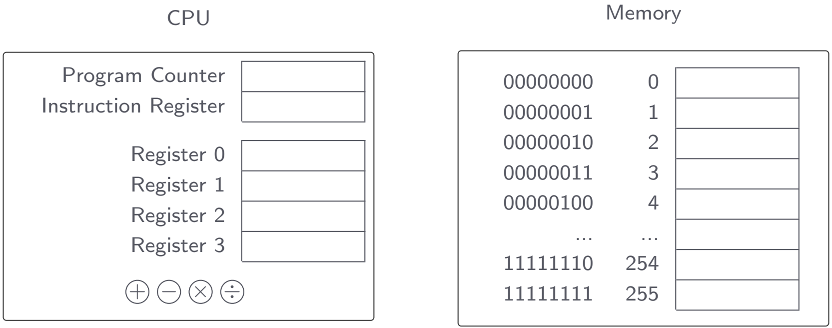
and the equivalent machine language program

```
00 10 00 01
10 11 10 10
```

Von Neumann Architecture

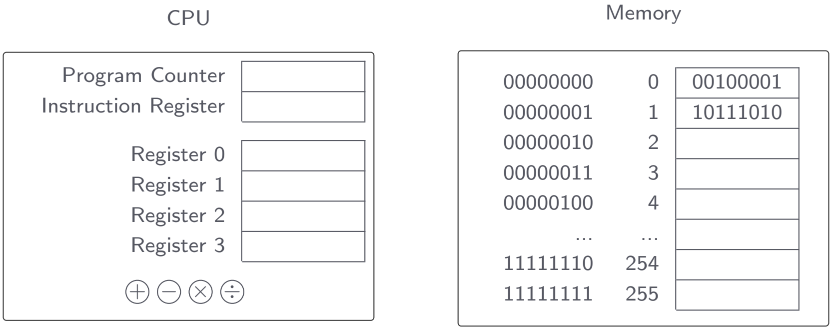
Von Neumann Architecture

Program execution



Von Neumann Architecture

Program execution



Program execution

CPU

Program Counter	
Instruction Register	
Register 0	00000100
Register 1	00000111
Register 2	
Register 3	

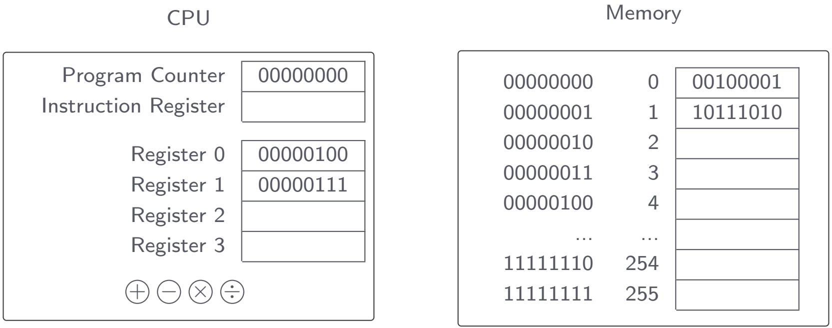
$\oplus$ $\ominus$ $\otimes$ $\div$

Memory

00000000	0	00100001
00000001	1	10111010
00000010	2	
00000011	3	
00000100	4	
...	...	
11111110	254	
11111111	255	

Von Neumann Architecture

Program execution



Von Neumann Architecture

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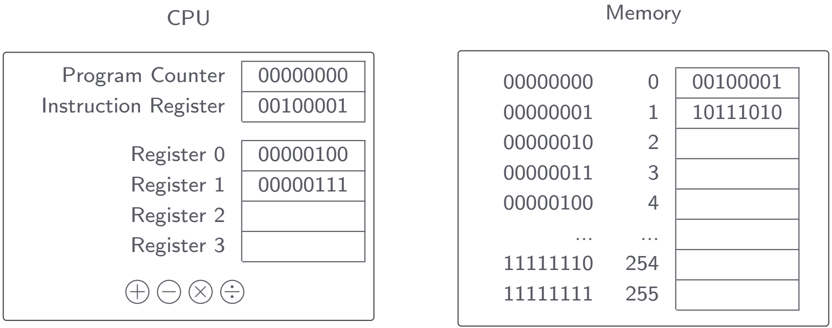

Von Neumann Architecture

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